REMARKS

Claims 1-77 were allowed in this application. However, claims 40-51 are being cancelled herein and will be presented in a continuation application. Claims 1-2, 8, 13-15, 18-19, 23, 28-30, 33, 35, 38, 52-55, 60-63, 71-74 have been amended. No new claims have been added.

A number of references have been previously made of record in a Supplemental Information Disclosure Statement dated Sept. 16, 2005 and received at the patent office on Sept. 19, 2005, as noted by the examiner in the Notice of Allowability. The following are comments on several of these references in relation to the claims presently standing in this application:

Aritome and claim 28 and 52

In paragraph 3 of the amended claims 28 and 52, the first boosting voltage level(s) are coupled to all of the transistors in the second string between said selected word line and the bit line connected to the second string to boost electrical potential(s) of channel regions of transistors in the second string to a value or values closer to the program voltage to reduce program disturb.

In Fig. 14(b) of Aritome, cell 2 is programmed by applying 0 volts to its gate, and by causing the channel region of cell 2 to be at a high voltage by applying 22 volts to its bit line (first bit line), thereby causing the cell to turn from a depletion mode to an enhancement mode. Thus, to inhibit the programming of a cell (cell A, not shown) connected to a second bit line addressed by the word line at 0 volts used to program cell 2, a low voltage of 10 volts is applied to the second bit line. Since the channel regions of the cells connected to the second bit line will remain at 10 volts despite the 22 volts applied to cells 7 and 8, the 22 volts applied to cells 7 and 8 will not raise the channel voltage of the cell A. Thus, there is no "boosting" of the channel region voltage. This is thus different from claims 28 and 52. Therefore, Aritome does not teach the application of boosting voltage(s) taught by claims 28 and 52.

US 2002/0110019 Satoh, US Patent 5,715,194 and claims 1, 13, 14

Claims 1 and 13, as amended, differentiate from Satoh. In the local self-boosting (LSB) scheme of Fig. 10, Satoh teaches that when the transistor MC13 (which is 3 storage transistors away from the bit line) addressed by WL 4 is programmed, 0 volts is applied to WL3 and Vpass is applied to WL1 and WL2. Therefore, the break down at the source side of transistor ST1 is not reduced, and may cause the charge state of transistor MC11 to change.

Claim 14 differs from Satoh for similar reasons, since the voltages applied when at least one of the two transistors programmed in sequence will be similar to those described above in reference to claims 1 and 13.

From Fig. 8 of the '194 patent, when transistor 104g' (which is 3 storage transistors away from the source line) is programmed, 2 volts is coupled to transistors 104j' and 104f' and 9 volts will be applied to word line 306d and coupled to transistor 104f". Therefore, the break down at the drain side of the select transistor in string 302a' addressed by word line 312'(SG_S) is not reduced, and may cause the charge state of the transistor in string 302a' addressed by word line 306d to change, unlike claims 1 and 13.

Claim 14 differs from the '194 patent for similar reasons, since the voltages applied when at least one of the two transistors programmed in sequence will be similar to those described above in reference to claims 1 and 13.

US Patent 5,715,194 and claims 28, 40, 52, 60 and 71

Claims 28 and 52 differ from '194 in that the '194 does not apply boosting voltage level(s) to all of the transistors between the selected word line and the bit line string to boost electrical potential(s) of channel regions of transistors in the string to be inhibited to a value or values closer to the program voltage to reduce program disturb. Thus, in both Figs. 5 and 8 of the '194 patent, 2 volts are applied to transistor 104h (Fig.

5) and transistors 104h' and 104h", which do not boost the electrical potential(s) of channel regions to a value or values closer to the program voltage to reduce program disturb.

In claim 60, voltage level(s) are applied to two sets of transistors on both sides of the selected word line (i.e. one used to program a transistor in a first string) and in a second string that is to be inhibited, so that at least one transistor in each set is turned off. Claim 60 differs from the '194 patent in that the voltage level(s) are such that when at least one of such voltage level(s) is coupled to an unprogrammed transistor in the first string, it will be turned on, but when it is coupled to a programmed transistor, it will be turned off.

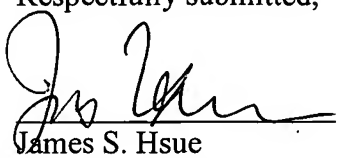
In the '194 patent, such voltage level used in local self-boosting is deliberately chosen so that a transistor in such string (i.e. a string that is not inhibited) will be turned on whether or not it is programmed. For example, 2 volts is chosen to be applied to transistor 104g in Fig. 5 to make sure that it will be on whether or not it is programmed.

Claim 71 differs from the '194 patent since a voltage at or about 0 volts is coupled to at least one transistor in the string to be inhibited, in combination with other features in the claim.

Therefore, it is deemed this application is further allowable as presented herewith and an early indication of allowability is earnestly solicited. However, if the Examiner is

aware of any additional matters that should be discussed, a call to the undersigned attorney at: (415) 318-1162 would be appreciated.

Respectfully submitted,



December 28, 2005
Date

James S. Hsue
Reg. No. 29,545

PARSONS HSUE & DE RUNTZ LLP
595 Market Street, Suite 1900
San Francisco, CA 94105
(415) 318-1160 (main)
(415) 318-1162 (direct)
(415) 693-0194 (fax)